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Verification Engineer, 3+Years of Experience

**PROFESSIONAL SYNOPSIS:**

* Experience 5.6 years in Verification and Test benches in System Verilog and UVM.
* Working with Sevitech UST and deployed to the client intel for UX ip verification for transceiver serdes.
* Worked with **Smartsocs solutions private limited** and deployed in NXP semiconductors as contractor working on soc project from October 2021 till January 2022.
* Worked with with cientra tech solutions pvt ltd (Qualcomm client) from April 2021.
* Worked as Verification Engineer in SeviTech systems pvt ltd (A UST global company )from 4th July 2019 till 31st March 2021.
* Worked as Verification Engineer in INCISE infotech (Noida) from 29th august 2019 till 30th June 2019.
* Knowledge of **AHB,AXI4,Ethernet, APB,SPI, I2C protocol**.
* Knowledge of Code Coverage and Functional Coverage.
* Knowledge of **AHB, SPI, I2C.**
* Experience in SOC (communication Protocols) projects like **SPI, I2C .**
* Knowledge on ARC Processor and SOC verification concepts .
* Proficient in shell scripting .My work involves writing shell scripts to run multiple test case at a time to speed up the process, writing shell scripts to optimize gate level simulation .Updated makefile as 3 folds at run times as per the requirement.
* Writing shell scripts to run multiple test cases at a time to speed up the process.
* Working experience in perl basics ,perl arrays ,scalars,hashes, perl files and IO,regular expressions and subroutines.
* Worked as trainee engineer in **CoreEL technology** for more than one year involving in designing and verifying different design from scratch.
* Worked as research fellow in **IIT BHUBANESWAR** for more than two years in a research project under Sponsored research and industrial consultancy **(SRIC),IIT** **Bhubaneswar** , where I worked in the project “ a vehicle mounted surveillance system for tracking and monitoring the vehicle position and its surroundings”.

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| Client name | Parent company | Duration of work | Project name |
| INTEL | Sevitech UST | July 2022-Jan 2023 | UX IP , Trasnsciever serdes(Ip level) |
| NXP semiconductors | Smartsocs | October 2021-May 2022 | Secure car access (SOC level project) |
| Qualcomm | CIentra Techsolutions | April 2021-september 2021 | Camera soc and post silicon validation |
| SiliconWork(South korea) | UST | Feb 2020-April 2021 | Apple display subsystem project,Memory controller project |
| STmicroelectronics | UST | July 2019-Feb 2020 | SAR ADC |
| US client | Incise infotech | Jan 2019-June 2019 | Set up box soc |
| Europe client | Incise infotech | Aug 2018-Jan 2019 | AHB , GLS |

**PROJECTS:**

**Project : UX IP verification(Intel Client)**

UX quad is a form of serdes architecture .UX quad is a hard macro inside HSSI subsystem.It includes 4 instances of serdes phy hard ip,clockrx hard ip and various additional modules.

* + Tools used: verdi
  + Responsibilities:
    - Listing down features, scenarios
    - Testplan development
    - Test case coding
    - Coding Testbench components including reference model and checkers.Verification closure using Functional coverage & code coverage as closing criteria

**Project : LTS(Long tail support) for four SOCs and Camera module in Fillmore and Lemans SOC:(April-September 2021):**

**Description:**

**LTS:**

System on chips after tape out require support at times when it comes to critical functionality and updates, having the existing testing and verification environment ready and functioning with pre-existing text stimulus, so that it can support for future requirements.

**CAMSS:**

Verifying the camera module with additional features with pre-existing test suit and debugging build failures , assertion failures , data mismatch for Lemans and Fillmore soc.

Role:

1.Setting up development view and running with RTL sanity and VECTOR mode regression. (LTS)

2.Creation of smoke list for further regression analysis (LTS).

3.Creating config files for RadagastAU soc and running in latest baseline

4.Running separate test by creating development view which includes frequency plan and nominal tests. (Camera)

5.Debuging build failures (Camera)

6. Making toggle coverage 100 %(Camera)

7.Creating non tile and tile-based development view (Camera)

**Key challenges:**

1. 100 %Toggle coverage for Fillmore soc. (Camera)

2. Fixing file mismatch from one to another server. (LTS)

**Achievements:**

**1.**Fillmore soc was ready for tape out after reaching critical milestone of 100 % toggle coverage.

* **Memory Controller Functional Verification using System Verilog(Feb 2020-March 2021)**
  + Description:
    - Design supports SDRAM, SSRAM, Flash & Synchronous Chip select devices. It has support for 8 chip selects. It also supports flexible timing configuration for different memory types. As part of this design verification, we created testbench using SV to generate scenarios targeting all types of supported memories for different possible combinations & different sizes supported. We also developed monitor, reference model & checker as part self checking testbench implementation.
  + Tools used: ncsim
  + Responsibilities:
    - Listing down features, scenarios
    - Testplan development
    - Developing testbench architecture
    - Coding Testbench components including reference model and checkers
    - Verification closure using Functional coverage & code coverage as closing criteria.

**ADCQ subsystem verification: (Client :STmicroelctronics)**

**July -Feb 2020)**

**HVL/HDL :**System Verilog

**TB Methodology :**UVM

**EDA Tools :**Cadence Xcelium , SimVision, IMC,vManager

ADCQ Subsystem aims at providing SW defined measurement sequences to CTU Interface of SARADC Digital Interface (SARADC).

ADCQ Subsystem consists of two modules:

• Queue

• ADCXBAR module

Different Queue can provide measurement sequences through independent paths to ADCXBAR, which in turn provides these commands to CTU IF of SARADC on basis of ADCQ priority definition.

Queue consists of one command queue (CMDQ) and one data queue (DATAQ) combined as a logical unit. Both the CMDQ and DATAQ are implemented using FIFO architecture. In one ADCQ Subsystem, up to four Queues can be instantiated. Queue interacts with ADCXBAR through QBUS protocol.

**Responsibilities:**

* Understood the ADCQ subsystem Specification and devised a test plan.
* Made class based verification environment in UVM.

**GLS(Gate level simulation):US client -Dec 2018-April 2019**

**HVL/HDL:** System Verilog

**TB Methodology**: UVM

**EDA Tools:** Cadence NCSim, SimVision

**Description:**Base band processor having more than 10 million gates design (elendil top). The design contains analog blocks, Ethernet ,memories,multiple DMAs,USB,SPI blocks. My job is to do the gate level simulations and clean-up all the driver’s and checker’s of RTL testbench as the initial TB has internal signal probing at multiple places.

**Responsibilities:**

* Testbench cleanup and fixing the RTL and Gate level TB mismatches
* Correcting the checkers
* Debugging the multi million gates design.
* Simulating the test case for GLS with SDF.

**Key Challenges and Identified Issues:**

* Non-resetable flops, Dual port memories (simultaneously access), Huge delay in pre SDF and reset timing bugs etc.
* Debugging on optimized netlist.
* The dump size is very huge and debugging and tracing the signals requires much more time.
* Studied questasim gate level optimization methods and get it implemented on latest simulation environment reducing the simulation time 3 days to 1 day with optimized netlist.
* Got all memories initialized and also corrected internal probing in the checkers.
* Identified zero delay glitches causing simulation go wrong in the Riviera environment , causing simulation failure and data mismatch.

**SOC verification: I2C peripheral subsystem (Sept 2018-Nov 2018)**

**HVL/HDL :**System Verilog and C

**TB Methodology :**Verilog

**EDA Tools :**Cadence NCSim, SimVision, IMC

**Description:** I2C (Inter-IC) is a 2-wire serial interface protocol with ARC770D processor. On SOC I2C functions as master only, in two modes: normal and fast, allows clock stretching. Command and data FIFOs enable process of transmit, receive using standard external signals Serial clock (SCL) and Serial Data (SDA). Operation initiates with a start bit, address, read/write operation, ack, data and terminates at stop bit. I2C interfaces with AMBA APB on SoC.

**Responsibilities:**

* Understood the SOC-I2C Specification.
* Understood booting process and interrupt handling.
* Developed C test cases to verify the BUS and Interrupts.
* Verify connectivity between I2C and processor .
* Understood SOC Test Bench Architecture and verification environment.

**SOC verification: SPI peripheral subsystem(June 2018 to August 2018)**

**HVL/HDL :**System Verilog and C

**TB Methodology** : Verilog

**EDA Tools :**Cadence NCSim, SimVision, IMC

**Description:** This project deals with SoC verification of SPI with ARC770D processor. A full duplex serial peripheral interface consists of 4-wire signals interfacing SPI slave, using Chip select, serial clock, serial data input and serial data output. SPI on SoC is interfaced with APB bus. Polarity and phase of serial clock is programmable. Worked on Interrupt Handling, generation of Interrupt, execution of ISR (IP to Processor connectivity) and serving the interrupts.

**Responsibilities:**

* Reading SoC-SPI Specification.
* Understanding SoC Testbench Architecture and Verification environment.
* Created C test cases to verify the BUS and Interrupts.
* Verify connectivity between SPI, processor.
* Understood booting process and Interrupt handling.

**SOC Verification of GMAC Ethernet**

**HVL/HDL-** System Verilog

**TB Methodology-**Verilog

**Tools used-** Cadence Ncsim, Simvision

**Description-** GMACEthernet is the traditional technology for connecting wired LANs, enabling devices to communicate with each other via a protocol a set of rules or common network language**.** This project deals with SOC verification of Ethernet registers with ARC processor. It has two GMAC instances GMAC0 and GMAC1.

**Responsibilities:**

* Under the concept of GMAC ethernet and its frame structure.
* Read the specification and register configurations.
* Write C test cases for checking the speed and burst length.
* Verify the connectivity between processor and GMAC1 instance.

**AMBA APB Bus Protocol Verification using UVM(Jan2018-Mar2018)**

**HVL/HDL :** System verilog

**TB Methodology** : UVM

**EDA Tools :** Cadence NCSim, SimVision, IMC

**Description**: The AMBA APB protocol is targeted at low-performance, suitable for low-frequency system designs.

**Responsibilities:**

* Understand specifications and devised a test plan.
* Made class based Verification environment in UVM.

**AMBA AHB Bus Protocol Verification using UVM(Oct 2017-Dec 2017)**

**HVL/HDL :** System verilog

**TB Methodology :**  UVM

**EDA Tools :** Cadence NCSim, SimVision, IMC

**Description**:The AMBA AHB protocol is targeted at high-performance, high-frequency system designs and includes a number of features that make it suitable for a high-speed data transfer.

**Responsibilities:**

* To verify AHB protocol features Burst transfer, aligned address,pipelined operations and verify AHB Slave.
* Understand specifications and create test plan.
* Test case for verifying the design.

**Asynchronous FIFO: ( Jan 2017-Sep 2017)**

Design of an Asynchronous First-In-First Out memory queue with control logic that performs management of the read and write pointers, generation of status flags like almost empty and almost full, and optional handshake signals for interfacing with the user logic.

Software Tools: QuestaSim & Vivado. Hardware: Xilinx Zedboard

**Round Robin Arbiter: (July 2016-Dec 2016)**

Round Robin Arbiter: The aim of this project was to develop a Round Robin Arbiter to help schedule the processes/requests of four entities cyclically in a given priority order so as to ensure execution of all the requests in a cycle. The major blocks of this design are the Acknowledgement Register Block, Priority Logic, Feedback Logic and Output Logic. The priority assigned to the four entities is user defined and can be varied according to the requirements.

Software Tools: QuestaSim & Vivado. Hardware: Xilinx Zedboard

**Research fellow, Indian Institute of Technology, Bhubaneswar**

Worked as project fellow in IIT Bhubaneswar (School of mechanical sciences) in a technical project of MHRD (Govt of India) under the guidance of Prof Dr Satyanarayana Panigrahi (Ph.D., IISC, Bengaluru). o Project titled “A vehicle mounted surveillance system for tracking and monitoring the vehicle positions and its surroundings “. o In the above project a Raspberry pi model B+ and various other processors like Arduino, were used for certain testing purposes. o Knowledge in python language while working with Raspberry Pi computer was required.

**EDUCATIONAL QUALIFICATION**

* **B.Tech.** in ETC From SILICON INSTITUTE OF TECHNOLOGY (B.P.T.U) in 2013 with 63.5%.